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Remarks

Applicant and his representatives wish to thank Examiner Chen for the thorough examination of the present application and the detailed explanations in the Office Action dated July 3, 2006. Support for the amendments to claims 1, 2, 3, 5, 6, 8, 9, 11, 15, 16 and 18 can be found in the specification in paragraphs [0030]-[0031] and [0033] and in claims 1, 2, 3, 5, 6, 8, 9, 11, 15, 16 and 18 and FIGS. 2C and 2D as originally filed. Support for new claim 21 can be found in the specification in paragraph [0024]. Support for new claim 22 can be found in the specification in paragraph [0030]. Thus, no new matter is introduced by the present amendment.

The present invention relates to a method of forming a trench in a semiconductor device, including the steps of (a) forming a polish stop layer on a semiconductor substrate, (b) forming an organic anti-reflection coating on the polish stop layer, (c) selectively etching the anti-reflection coating to form an anti-reflection coating pattern, (d) etching the polish stop layer and the semiconductor substrate such that ends of the polish stop layer adjacent to the trench are rounded along substantially the entire thickness of the polish stop layer, and a trench having sloped sidewalls is formed to a predetermined depth, and (e) forming an insulation layer that fills the trench.

The Objection to the Amendment Filed September 16, 2005 under 35 U.S.C. § 132(a) and the Rejection of Claims 2-4, 8-10 and 15-17 under 35 U.S.C. § 112, first paragraph

The objection to the Amendment filed September 16, 2005 under 35 U.S.C. § 132(a) and the rejection of claims 2-4, 8-10 and 15-17 under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement is respectfully traversed.

The Amendment filed September 16, 2005 does not introduce new matter. Rather, the Amendment filed September 16, 2005 is supported by the original disclosure.

The Amendment filed September 16, 2005 added the phrase "or more" to claims 2, 4, 8, 10, 15 and 17, and deleted the phrase "one of" from claims 3, 9 and 16. However, as is

established by the accompanying Declaration under Rule 1.132 of Young-Hun Seo, one skilled in the art of semiconductor processing and/or manufacturing understands that the subject matter of these claim amendments is disclosed by the specification as originally filed (see, e.g., paragraphs 15 and 17 of the accompanying Declaration of Seo).

For example, the present specification discloses:

- "Dry etching" the silicon nitride (polish stop) film 13, the pad oxidation layer 12 and the semiconductor substrate 11 form a trench 100 (see paragraph [0030], p. 7 of the application as originally filed); and
- Forming "a sidewall polymer" during dry etching (see paragraph [0033], p. 8 of the application as originally filed).

These disclosures encompass mixtures of the etchants recited in claims 2-4, 8-10 and 15-17. Thus, claims 2-4, 8-10, and 15-17 as filed September 16, 2005 are supported by the specification as originally filed (see, e.g., paragraph 17 of the accompanying Declaration of Seo).

For example, one skilled in the art understands that forming a sidewall polymer occurs when dry etching SiO_2 (e.g., a material suitable for pad oxidation layer 12) and silicon nitride (SiN; a material suitable for polish stop layer 13) with a fluorocarbon plasma (see, e.g., Wolf, "Silicon Processing for the VLSI Era," vol. 1, pp. 672-673 and 678-683, particularly p. 672, Table 14-2; p. 678, Fig. 14-17 and the first paragraph therebelow; p. 680, Fig. 14-19(b) and paragraph #2; and p. 683, lines 3-4, the first full paragraph, and Fig. 14-23; see Exhibit A of the Declaration of Seo). Notably, Wolf teaches the well-known formation of sidewall polymer in a process that etches a trench into silicon under a layer of SiO_2 (a well-known structure resulting from the oxidation of silicon) using a mixture of CHF_3 and CF_4 (both of which are recited in claims 2-4, 8-10 and 15-17), or a mixture of a fluorocarbon and O_2 (see paragraph 18 of the accompanying Declaration of Seo and Exhibit A thereto [Wolf], p. 683, the first paragraph, ll. 11-16, and Fig. 14-23).

It is known in the art that a very similar sidewall polymer is formed when etching silicon nitride (a well-known mask layer for etching a trench into a silicon substrate) with fluorocarbon-

based etchant. Therefore, one skilled in the art(s) of semiconductor devices and semiconductor manufacturing would readily understand that the present specification inherently discloses and supports dry etching a silicon nitride (polish stop) layer and a semiconductor substrate using a mixture of the etchants recited in claims 2-4, 8-10 and 15-17 above, notably a mixture of the CHF_3, CF_4 and/or O_2 etchants (see paragraph 19 of the accompanying Declaration of Seo).

O_2 itself does not dry etch silicon nitride, SiO_2 or Si (see paragraph 20 of the accompanying Declaration of Seo and Wolf, p. 672, Table 14-2, attached as Exhibit A thereto). As a result, one skilled in the art would understand that, to the extent O_2 is used in the etching step recited in claims 2-4, 8-10 and 15-17, the silicon nitride (polish stop) film 13, the pad oxidation layer 12 and the semiconductor substrate 11 must be etched with a mixture of O_2 and another etchant (e.g., CF_4; see the accompanying Declaration of Seo Wolf, p. 673, first paragraph of section 14.4, and Table 14-2 on p. 672, attached as Exhibit A thereto). Any disclosure to the effect that silicon nitride, SiO_2 or Si is dry etched with O_2 alone is an error that is readily apparent to those skilled in the art (see paragraph 20 of the accompanying Declaration of Seo). As a result, one skilled in the art(s) of semiconductor devices and semiconductor manufacturing would further understand that the present specification application as originally filed discloses dry etching a silicon nitride (polish stop) layer 13 and a pad oxidation layer 12 to form a trench in a semiconductor substrate using a mixture of the etchants including CF_4, CHF_3, and/or O_2 as recited in claims 2-4, 8-10 and 15-17 above (see paragraph 21 of the accompanying Declaration of Seo).

In addition, the present specification discloses that the antireflection coating ARC 14 may be a conventional ARC made of an organic material (p. 7, l. 7-8), and that dry etching to form the trench 100 can be controlled such that a small amount of exposed ends of the ARC layer 14 is removed (p. 7, l. 20-p. 8, l. 1; see paragraph 22 of the accompanying Declaration of Seo). As is known in the art, dry etching an organic solid (such as the embodiment of the ARC 14 disclosed by the present specification and discussed in this paragraph) can be done with O_2 alone or in combination with CF_4 (see paragraph 23 of the accompanying Declaration of Seo and Wolf, p. 672, Table 14-2, Exhibit A to the accompanying Declaration of Seo). As a result, one skilled

in the art(s) of semiconductor devices and semiconductor manufacturing would understand that the present specification supports dry etching an organic ARC using one or more of the etchants recited in claims 2-4, 8-10 and 15-17 (paragraph 23 of the accompanying Declaration of Seo). Thus, the present application as originally filed inherently discloses etching an organic antireflection coating using a mixture of the O_2 and CF_4 etchants recited in claims 2-4, 8-10 and 15-17.

Even further, one skilled in the art understands that *molecular* gases are used in dry etching (see paragraph 24 of the accompanying Declaration of Seo and Wolf, pp. 668-9, particularly p. 669, l. 7, attached thereto as part of Exhibit A). One of the gases recited in claims 2-4, 8-10 and 15-17, Ar (argon), is not a molecular gas (paragraph 24 of the accompanying Declaration of Seo). Accordingly, one skilled in the art understands that Ar is not used alone in dry etching (see paragraph 24 of the accompanying Declaration of Seo and Wolf [Exhibit A thereto], p. 679, the second full paragraph, which teaches the well-known use of Ar ions to *assist* dry etching processes). One skilled in the art therefore understands that dry etching uses a molecular gas such as CHF_3, CF_4, O_2, or HeO_2, and as a result, the disclosure of Ar as a gas for use in dry etching must refer to its use in combination with one (and possibly more) of the molecular gases recited in claims 2-4, 8-10 and 15-17 (see paragraph 24 of the accompanying Declaration of Seo). Any disclosure to the effect that silicon nitride, SiO_2 or Si is dry etched with Ar alone is an error that is readily apparent to those skilled in the art (see paragraph 24 of the accompanying Declaration of Seo).

Thus, the present application as originally filed inherently discloses etching a polish stop layer, a pad oxidation layer and/or a semiconductor substrate using a mixture of Ar and at least one of the CHF_3, CF_4, O_2, and HeO_2 etchants recited in claims 2-4, 8-10 and 15-17 (see paragraph 25 of the accompanying Declaration of Seo).

Without doubt, the present specification discloses dry etching with a single gas (see paragraphs [0014] and [0031], pp. 4 and 7-8 as originally filed, respectively). Consequently, those skilled in the art would readily understand that the above-identified application discloses and conveys dry etching the organic antireflection coating 14, the silicon nitride (polish stop)

film 13, the pad oxidation layer 12 and the semiconductor substrate 11 using one or more of the gases recited in claims 2-4, 8-10 and 15-17.

To the extent that the disclosures in paragraphs [0014] and [0031] of the present specification of certain gases as dry etching agents alone are considered erroneous, the Amendment filed September 16, 2005 corrects readily apparent errors in the disclosure. Correction of an error is not new matter if one skilled in the art would appreciate not only the existence of an error, but what the error is. *Koito Mfg. Co. v. Turn-Key-Tech. LLC*, 381 F.3d 1142; 72 U.S.P.Q.2D 1190 (Fed. Cir. 2004), citing *In re Oda*, 58 C.C.P.A. 1353, 443 F.2d 1200, 1206 (C.C.P.A. 1971). As discussed above and in the accompanying Declaration of Seo, one skilled in the art would readily ascertain that any disclosure limiting dry etching the silicon nitride (polish stop) film 13, the pad oxidation layer 12 and the semiconductor substrate 11 to a single gas is erroneous in certain cases (e.g., O_2 and Ar). Thus, to the extent paragraphs [0014] and [0031] of the disclosure are considered to contain one or more errors, correction of such errors is not new matter.

Furthermore, as discussed above, the specification as originally filed supports an amendment reciting dry etching with a mixture of the more than one of the gases. Because the amended subject matter is inherently contained in the originally-filed application, it does not constitute new matter. *Koito Mfg. Co. v. Turn-Key-Tech*, citing *Schering Corp. v. Amgen Inc.*, 222 F.3d 1347, 1352 (Fed. Cir. 2000). Thus, no new matter was introduced by the Amendment filed September 16, 2005.

Therefore, this ground of rejection should be withdrawn.

The Rejection of Claims 1-6 and 8-20 under 35 U.S.C. § 103(a)

The rejection under 35 U.S.C. § 103(a) of Claims 5, 11 and 18 as being unpatentable over Moore et al. (US 6,884,725) in view of Bamnolker et al. (US 6,890,859) is respectfully traversed.

Moore et al. discloses a method of forming a trench in a semiconductor device, where the method includes forming a polish stop layer on a semiconductor substrate, etching the polish

stop layer and etching the semiconductor substrate to a predetermined depth to form a trench, and forming an insulation layer that fills the trench. However, Moore et al. fails to disclose or suggest the steps of forming an organic anti-reflection coating on the polish stop layer, etching the polish stop layer such that ends of the polish stop layer adjacent to the trench are rounded along substantially the entire thickness of the polish stop layer, or etching the semiconductor substrate to a predetermined depth to form a trench that has sloped sidewalls, as recited in Claim 1 above.

Moore et al. disclose in FIG. 10 a wafer fragment 10a that comprises a substrate 12, a pad oxide layer 14, and an etch-stop layer 16 overlying oxide layer 14. Etch-stop layer 16a can comprise, for example, silicon nitride. Nitride-containing etch-stop layer 16 has been subjected to a facet etch to reduce a sharpness of corners 22 (FIG. 5). Specifically, etch-stop layer 16a (FIG. 10) comprises a facet 50 in place of corner 22 (FIG. 5), and has effectively replaced corner 22 with a pair of corners 52 and 54. Each of corners 52 and 54 comprises an angle greater than the about 90° angle of corner 22 (FIG. 5). Accordingly, the facet-etching of the exemplary first embodiment processing has effectively removed a portion of upper corner 22 (FIG. 5) to reduce a sharpness of the corner angle from a first degree (about 90°) to a second degree (an angle of greater than 90°; col. 4, ll. 20-46 of Moore et al.).

FIG. 12 of Moore et al. illustrates a semiconductor wafer fragment 10c at a processing step similar to the prior art processing step of FIG. 1. A difference between semiconductor wafer fragment 10c of FIG. 12 and wafer fragment 10 of FIG. 1 is that wafer fragment 10c comprises an etch-stop layer 16c having two distinct portions, whereas wafer fragment 10 comprises an etch-stop layer 16 containing only one portion. The two portions of etch-stop layer 16c are an upper portion 70 and a lower portion 72. Preferably, upper portion 70 has a faster etch rate when exposed to subsequent etching conditions than does lower portion 72. (Col. 6, ll. 24-33 of Moore et al.)

For example, in applications wherein etch-stop layer 16c comprises nitride, upper portion 70 can comprise $Si_xN_yO_z$, wherein x, y and z are greater than zero, and lower portion 72 can consist essentially of SiN. Upper portion 70 will then etch faster relative to lower portion 72

under subsequent etching conditions comprising exposing nitride-containing layer 16c to hydrofluoric acid. (Col. 6, ll. 33-39 of Moore et al.) Thus, regardless of whether Moore et al. recite any anti-reflective properties for upper portion 70, Moore et al. do not disclose an organic antireflection coating, as recited the present Claim 1.

Furthermore, each opening 20 in substrate 12 shown in FIGS. 3-5, 10-11 and 13-14 of Moore et al. has straight sidewalls. Moore et al. do not affirmatively disclose any openings 20 in substrate 12 that have sloped sidewalls, either in the Figures or in the specification. Similarly, Moore et al. do not affirmatively disclose any examples or alternatives of etch-stop layer 16 or lower nitride portion 72 that have ends that are rounded along substantially the entire thickness of the layer, either in the Figures or in the specification.

Thus, Moore et al. fails to disclose the steps of forming an organic anti-reflection coating or etching a polish stop layer such that it has ends that are rounded along substantially the entire thickness of the layer, or etching the semiconductor substrate to form a trench that has sloped sidewalls, as recited in Claim 1. As a result, Moore et al. is saliently deficient with regard to Claim 1.

Bamnolker et al. fail to cure all of the deficiencies of Moore et al.

Bamnolker et al. disclose a method for forming a trench in a semiconductor substrate, which has a silicon layer, an oxide layer overlying the silicon layer, and a nitride layer overlying the oxide layer (Abstract, ll. 1-4). The method includes etching the nitride layer to a nitride end point using a nitride etching chemistry, which includes a fluorinated hydrocarbon, oxygen, and an inert gas selected from the group consisting of neon, argon, krypton, xenon, and combinations thereof (Abstract, ll. 4-8). However, neither nitride layer 8 (col. 1, ll. 21-40 and FIGS. 1-3) or nitride layer 30 (col. 3, ll. 60-67; col. 4, ll. 26-40; and FIG. 6) appear to have ends that are rounded along substantially the entire thickness of the layer. Thus, Bamnolker et al. fail to cure all of the deficiencies of Moore et al. with regard to the present Claim 1.

The method of Claim 1 provides improved results (e.g., a trench-fill capability) that are not disclosed, suggested or appreciated by Moore et al. and Bamnolker et al. (see paragraph 5 of the accompanying Declaration of Seo). For example, etching the polish stop layer such that ends

of the polish stop layer are rounded along substantially the entire thickness of the polish stop layer enables filling a relatively narrow trench in the substrate (e.g., fabricated using a semiconductor manufacturing process having a critical dimension of 0.18 μm or less) with an insulation layer using previous-generation trench-filling equipment (e.g., designed for manufacturing processes having a critical dimension of, e.g., 0.25 μm) in commercially acceptable yields (see paragraphs 6 and 13 of the accompanying Declaration of Seo).

Shallow trench isolation (STI) is frequently used to form isolation structures in a semiconductor device. In STI, a trench is formed in a semiconductor substrate, and an insulation material is filled in the trench. It is important in STI to completely fill the trench with the insulation material, without the formation of voids, which can lead to defects in the devices and reduced yields (see paragraph 7 of the accompanying Declaration of Seo; also see paragraphs [0002]-[0003] of the specification).

In semiconductor manufacturing processes having a critical dimension of 0.18 μm or less, one typically needs trench-filling equipment designed for filling trenches having a width at or near the critical dimension. The term "critical dimension" refers to a minimum design rule, or the minimum width for a structure or feature on the semiconductor device that can be reliably made using a given set of photolithography and other processing equipment (see paragraph 8 of the accompanying Declaration of Seo). Such trench-filling equipment adds considerable cost to the semiconductor manufacturing process, and consumes valuable floor space in a wafer fabrication facility ("fab") that is configured for manufacturing wafers using processes having a critical dimension of 0.18 μm or less, as well as manufacturing processes having a critical dimension of more than 0.18 μm (e.g., 0.25 μm; see paragraph 9 of the accompanying Declaration of Seo).

The benefit of using the same trench-filling equipment for both types of manufacturing processes (i.e., having a critical dimension of 0.18 μm or less, and having a critical dimension of, e.g., 0.25 μm) is commercially significant, in terms of reducing the cost of wafers manufactured on processes having a critical dimension of 0.18 μm or less, maximizing the investment in trench-filling equipment for manufacturing processes having a critical dimension of more than

0.18 μm (e.g., 0.25 μm), and maximizing efficiency of floor space in a fab configured for manufacturing wafers using both types of manufacturing processes (see paragraph 10 of the accompanying Declaration of Seo).

Based on the Declarant's knowledge of actual production data for manufacturing processes having a critical dimension of 0.18 μm or less, etching the polish stop layer such that ends of the polish stop layer are rounded along substantially the entire thickness of the polish stop layer enables filling a trench in the substrate with an insulation layer using trench-filling equipment designed for manufacturing processes having a critical dimension of more than 0.18 μm (e.g., 0.25 μm) in commercially acceptable yields (see paragraph 11 of the accompanying Declaration of Seo).

Based on the Declarant's knowledge of data generated during development of a manufacturing process having a critical dimension of 0.18 μm, etching the polish stop layer such that ends of the polish stop layer are not significantly rounded results in an unacceptably high incidence of void formation when filling a trench in the substrate with an insulation layer using trench-filling equipment designed for manufacturing processes having a critical dimension of more than 0.18 μm (e.g., 0.25 μm; see paragraph 12 of the accompanying Declaration of Seo). The defect rates in semiconductor devices manufactured using such etching and trench-filling steps are commercially unacceptable, and lead to commercially unacceptable yields (see paragraph 12 of the accompanying Declaration of Seo).

This difference in trench-filling capability between the method of Claim 1 and an otherwise comparable process in which ends of the polish stop layer are not significantly rounded is unexpected. In other words, prior to the present invention, one of ordinary skill in the art(s) of semiconductor processing and/or manufacturing would not have predicted that etching the polish stop layer such that ends of the polish stop layer are rounded along substantially the entire thickness of the polish stop layer would enable filling a trench in the substrate using a manufacturing process having a critical dimension of 0.18 μm with an insulation layer using trench-filling equipment designed for manufacturing processes having a critical dimension of

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more than 0.18 μm (e.g., 0.25 μm) in commercially acceptable yields (see paragraph 13 of the accompanying Declaration of Seo).

Thus, the method of Claim 1 provides unexpected improvements in trench-filling capability (using previous generation equipment, designed for a manufacturing process having a larger critical dimension than that of the process used to form the trench) that are not disclosed, suggested or appreciated by Moore et al. and Bamnolker et al. (see paragraphs 5, 6 and 13 of the accompanying Declaration of Seo). As a result, the present Claims 1-6 and 8-22 are fully patentable over Moore et al. and Bamnolker et al.

Consequently, this ground of rejection is unsustainable, and should be withdrawn.

Conclusions

In view of the above amendments and remarks, all bases for objection and rejection are overcome, and the application is in condition for allowance. Early notice to that effect is earnestly requested.

If it is deemed helpful or beneficial to the efficient prosecution of the present application, the Examiner is invited to contact Applicant's undersigned representative by telephone.

Respectfully submitted,

Andrew D. Fortney, Ph.D.
Reg. No. 34,600

401 West Fallbrook Avenue, Suite 204
Fresno, California 93711
(559) 432 – 6847